UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,467	03/30/2001	Carl D. Burch	10013968-1	5751

7590 01/13/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
GOLE, AMOL V	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/13/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/823,467	BURCH, CARL D.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/30/01, 9/20/01.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 3/30/01 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Receipt is acknowledged of the following papers:

1) Paper #2, IDS (9/20/01)

These papers have been placed of record in the file.

2. Claims 1-20 have been examined.

Specification

3. The abstract of the disclosure is objected to because the abstract may not exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: EARLY RETIREMENT OF INSTRUCTIONS NOT AFFECTING THE ARCHITECTURAL STATE OF THE PROCESSOR TO IMPROVE THROUGHPUT.

Claim Objections

5. Claims **1, 7, 8, 9, 17, 19 and 20** are objected to because of the following informalities:

a) Claims 1, 9, and 17 refer to "processing" instructions and stopping the "processing" of instructions in the various stages. However, it is understood from the drawings and description of the operation of the invention that the "issuing" of instructions will stop when the instruction queue is full and not the "execution and retirement" of the instructions. Hence, "processing" leads to some confusion and it is suggested that it be replaced preferably by "issuing" for purposes of clarity.

b) On line 2 of claims 7, 8, 19 and 20 the word "of" should be inserted between the words "processing the". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> *(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.*

7. Claims **1-20** are rejected under 35 U.S.C. 102(e) as being anticipated by Sheaffer (US006539471B2).

8. In regard to claim 1:

9. Sheaffer discloses a method for retiring instructions processed through various processing stages (fig. 6) including an instruction queue (Re-order Buffer (ROB), fig. 6), comprising the steps of:

processing the instructions until the instruction queue is full (decoded instructions are issued to the ROB [col. 5, lines 21-24]; although not explicitly mentioned, it is deemed inherent to the processor that instructions are processed until the ROB is full because if issuing is allowed the ROB may overwrite existing instructions and the processor would not work properly);

stopping processing the instructions in the various processing stages (although not explicitly mentioned, it is deemed inherent to the processor that when the ROB is full, the processing would be halted for correct operation of the processor);

for each instruction in the instruction queue, if the instruction meets the criteria for retirement (col. 5, lines 46-49), then

terminating the instruction (retires the instruction, col. 5., lines 46); and

updating a system processing the instruction to reflect that the instruction has been terminated (retires the instruction, col. 5., lines 46; retiring an instruction means committing the results to the architectural state, col. 1, lines 48-50).

10. In regard to claim 2:

11. Sheaffer discloses that decoded instructions are issued to the ROB [col. 5, lines 21-24]. Although it is not explicitly mentioned, it is deemed inherent to the Sheaffer method that after the instruction queue (ROB) is full, a step of requesting that instructions not be sent to the instruction queue is made because if issuing is allowed the ROB may overwrite existing instructions and the processor would not work properly.

12. In regard to claim 3:

13. Sheaffer discloses that the step of terminating further includes the step of removing the instruction from the instruction queue (retires the instruction, col. 5., lines 46; retiring the instruction involves removing it from the ROB).

14. In regard to claim 4:

15. Sheaffer shows that the various processing stages include one or more of the following stages: fetching, issuing, sorting, executing, queuing, and retiring (fig. 6).

16. In regard to claim 5:

17. Sheaffer further discloses that the instruction capable of early retirement includes an identification tag (stop bit [fig. 8]) for identifying whether the instruction is capable of early retirement (stop bit indicates whether the instruction can be retired without concern for the order of retirement [col. 5, lines 46-49]).

18. In regard to claim 6:

19. Although Sheaffer does not explicitly mention that NO-OP instructions, pre-fetch instructions, branch instructions, nullified instructions, and predicated-false instructions are identified as instructions capable of early retirement, this step is inherent to his processor because **all** instructions are identified as instructions capable of early retirement if their stop bit (fig. 8) is set accordingly (col. 5, lines 46-49).

20. In regard to claim 7:

21. Sheaffer further discloses that the criteria for early retirement are met when continued processing of the instruction does not change the architectural state of the system processing the instructions (the instructions for which the stop bit is set such that they can be retired early do not write to the architectural registers and hence do not change the architectural state of the system (col. 5, lines 46-49; col. 8, lines 20-22).

22. In regard to claim 8:

23. Sheaffer further discloses that the criteria for early retirement are met when continued processing of the instruction does not change the behavior of the program running the instruction (the results written are of instructions making up the program and hence do not cause the program to behave differently i.e. change its behavior. It should be noted that the applicant has not defined "change of behavior" within the claim itself

and hence it is interpreted as to cause the program to behave differently from that which is expected).

24. In regard to claims 9-16:

25. Sheaffer discloses the claimed elements of 9-16 as detailed in the rejection of claims 1-8 above. However, Sheaffer does not disclose a computer-readable medium embodying instructions that cause a computer to perform the method of claims 9-16 of the applicant's invention. But, it is deemed inherent to the method of Sheaffer that a computer-readable medium embodying instructions that cause a computer to perform the method of claims 9-16 because the processor is caused to perform this method when instructions are supplied to it.

26. In regard to claim 17:

27. Sheaffer discloses a system for retiring instructions processed through various processing stages (pipeline stages, fig. 6) including an instruction queue (ROB, fig. 6), comprising:

first processing means for processing the instructions until the instruction queue is full (decoded instructions are issued to the ROB [col. 5, lines 21-24]; although not explicitly mentioned, it is deemed inherent to the processor that instructions are processed by a first processing means until the ROB is full because if issuing is allowed the ROB may overwrite existing instructions and the processor would not work properly);

stopping means for stopping processing the instructions in the various processing stages once the instruction queue is full (although not explicitly mentioned, it is deemed inherent to the processor that when the ROB is full, the processing would be halted by a stopping means for correct operation of the processor);

second processing means for, for each instruction in the instruction queue if the instruction meets the criteria for retirement (col. 5, lines 46-49),

terminating the instruction (retires the instruction, col. 5., lines 46); and

updating a system processing the instruction to reflect that the instruction has been terminated (retires the instruction, col. 5., lines 46; retiring an instruction means committing the results to the architectural state, col. 1, lines 48-50).

28. In regard to claim 18:

29. Sheaffer discloses that decoded instructions are issued to the ROB [col. 5, lines 21-24]. Although it is not explicitly mentioned, it is deemed inherent to the Sheaffer method that after the instruction queue (ROB) is full, a requesting means requesting that instructions not be sent to the instruction queue is present because if issuing is allowed the ROB may overwrite existing instructions and the processor would not work properly.

30. In regard to claim 19:

31. Sheaffer further discloses that the criteria for early retirement are met when continued processing of the instruction does not change the architectural state of the

system processing the instructions (the instructions for which the stop bit is set such that they can be retired early do not write to the architectural registers and hence do not change the architectural state of the system (col. 5, lines 46-49; col. 8, lines 20-22).

32. In regard to claim 20:

33. Sheaffer further discloses that the criteria for early retirement are met when continued processing of the instruction does not change the behavior of the program running the instruction (the results written are of instructions making up the program and hence do not cause the program to behave differently i.e. change its behavior. It should be noted that the applicant has not defined "change of behavior" within the claim itself and hence it is interpreted as to cause the program to behave differently from that which is expected).

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty, which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections. See 37 CFR § 1.111.

a. Aho et al. ("Compilers Principles, Techniques, and Tools, " Addison-Wesley, pp. 530-531) describe dead-code optimization in compilers. It teaches that instructions that are dead, i.e. never subsequently used, can be safely removed.

b. Ronen (US005701442) teaches that NOP instructions have no architectural effect on the processor (col. 4 lines 66-67 col. 5, lines 1-2).

c. Thakkar et al. ("The Internet Streaming SIMD extensions", Intel Technology Journal, Q2, 1999) teaches that prefetch instructions don't update architectural state (pg. 3, col. 2, lines 1-2).

d. Ryan and Thompson report in "PowerPC 604 Weighs In," http://www.byte.com/art/9406/sec11/art1.htm, June 1994, that when the ROB is full, issue is stopped (pg. 3, lines 36-38).

e. Smith and Pleszkun ("Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. On Comp., Vol. 37, No. 5, May 1988, pp. 562-573) describe precise interrupts and the Reorder Buffer technique.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

AVG

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100